

DRAM Scaling & Bandwidth Challenges

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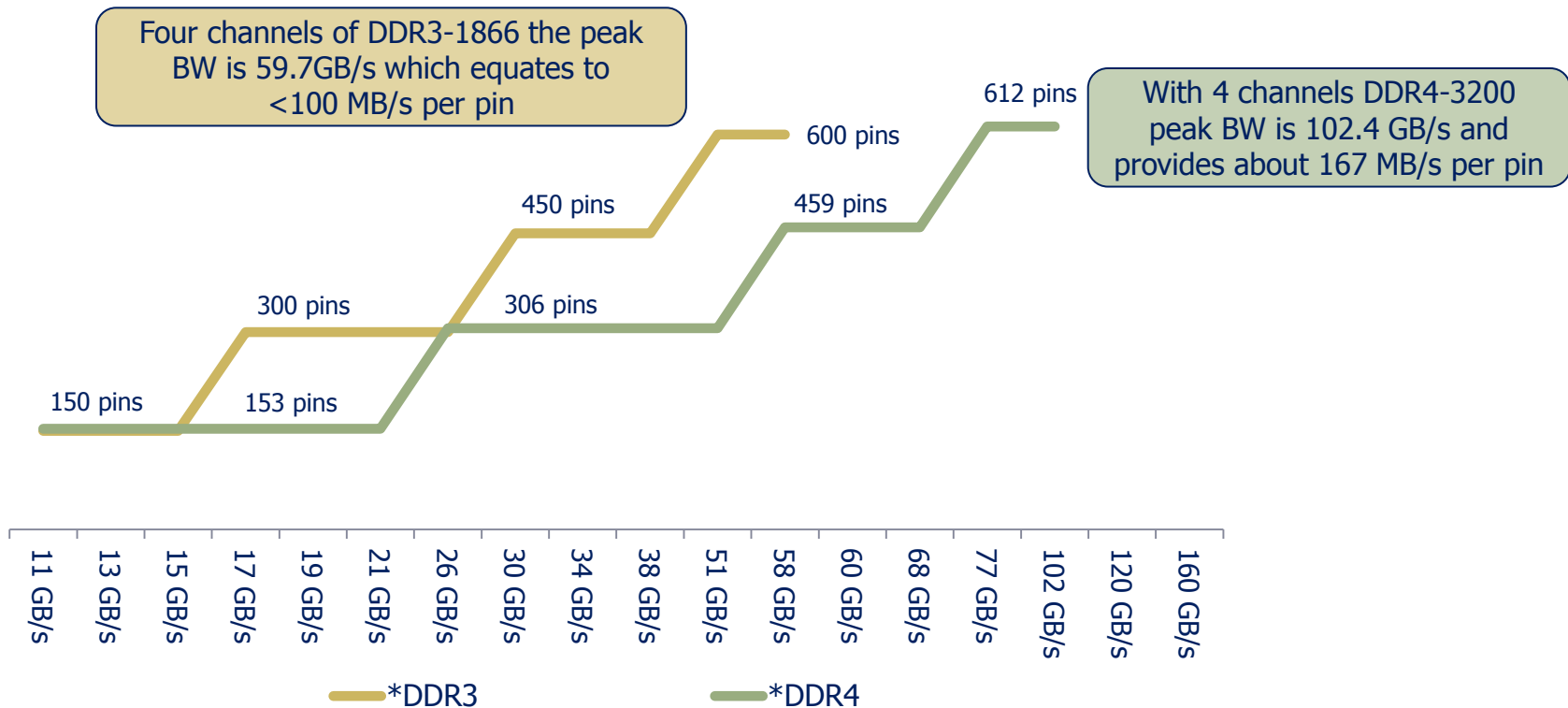
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Outline

- Bandwidth scaling roadmap
- Hybrid Memory Cube
- DRAM technology constraints
- Outlook for Photonics

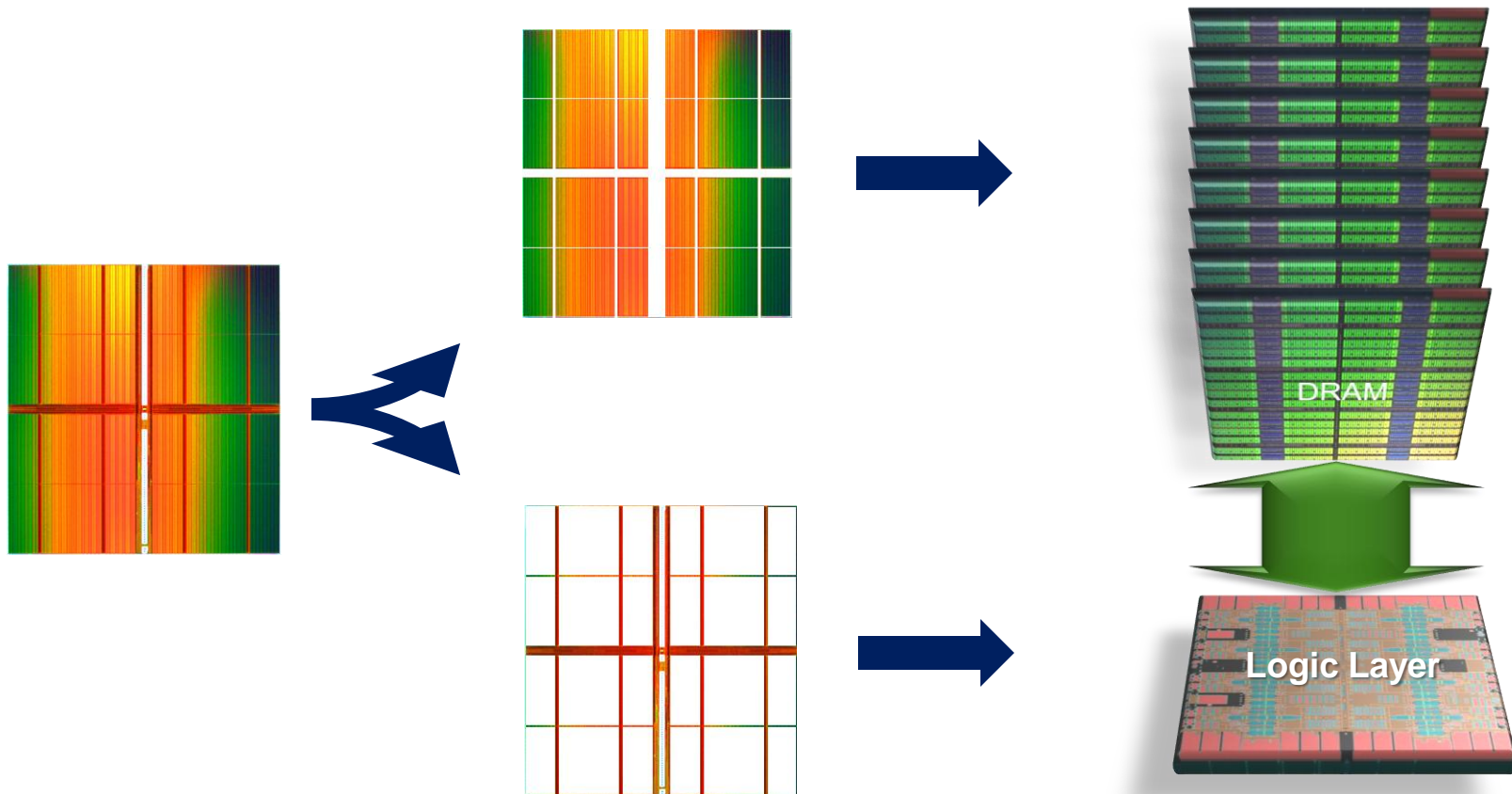
Bandwidth vs. pin count

- Performance (Bytes per second per pin)
 - HMC has the lowest pin count and has the highest BW



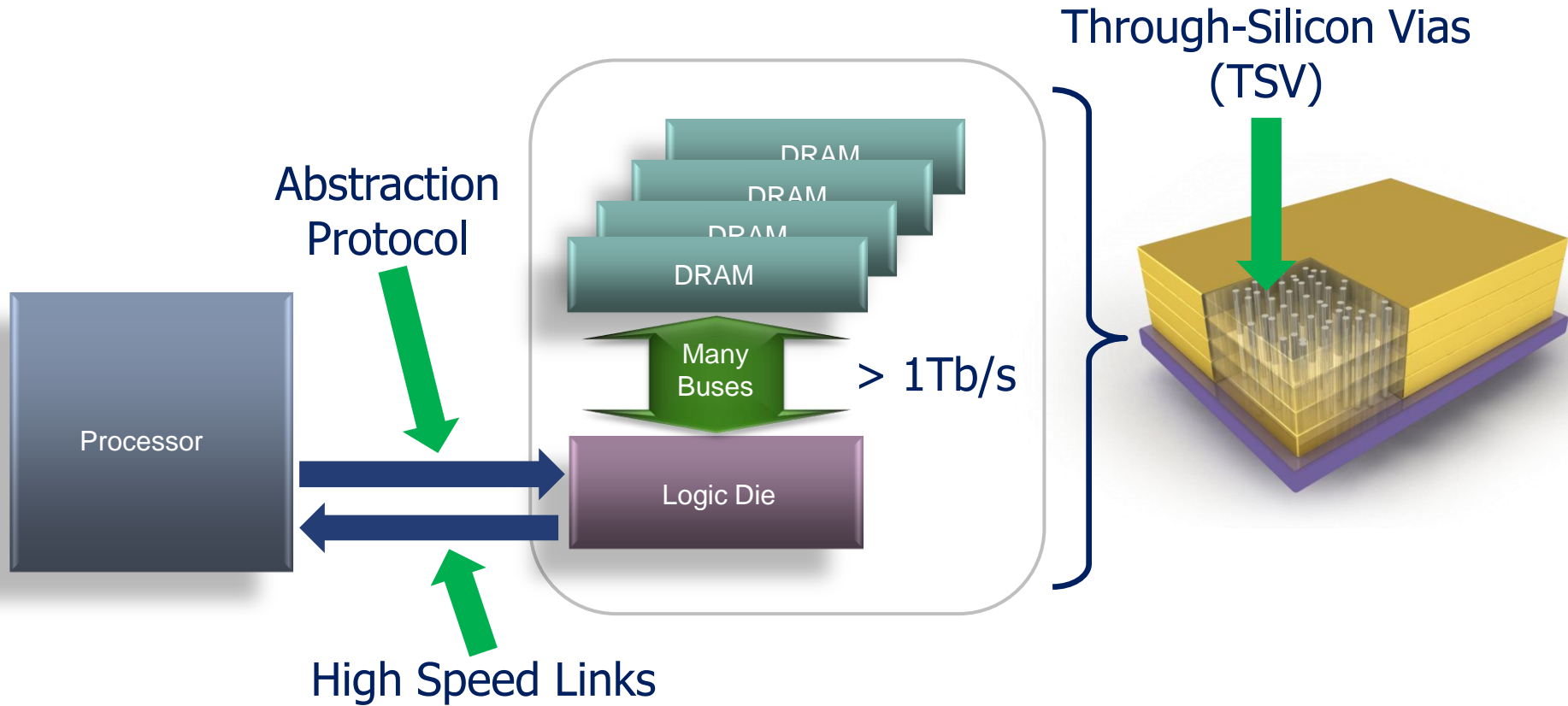
* For DDR3 and DDR4 bandwidth equals theoretical peak, all active pins listed.

Hybrid Memory Cube: DRAM Evolved



- Peripheral and Array on separate die
- Additional features available on logic layer

Hybrid Memory Cube (HMC)



Notes: Tb/s = Terabits / second
HMC height is exaggerated

<http://www.micron.com/innovations/hmc.html>

HMC_{Gen1}: Technology Demonstrator

Generation 1 (4 + 1 memory configuration)

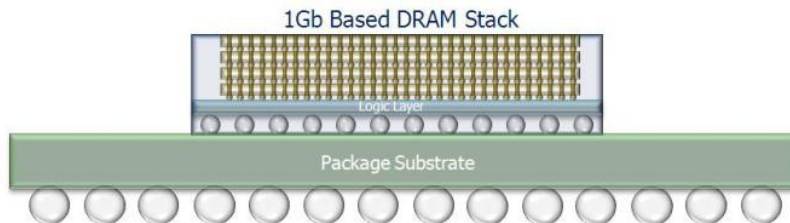
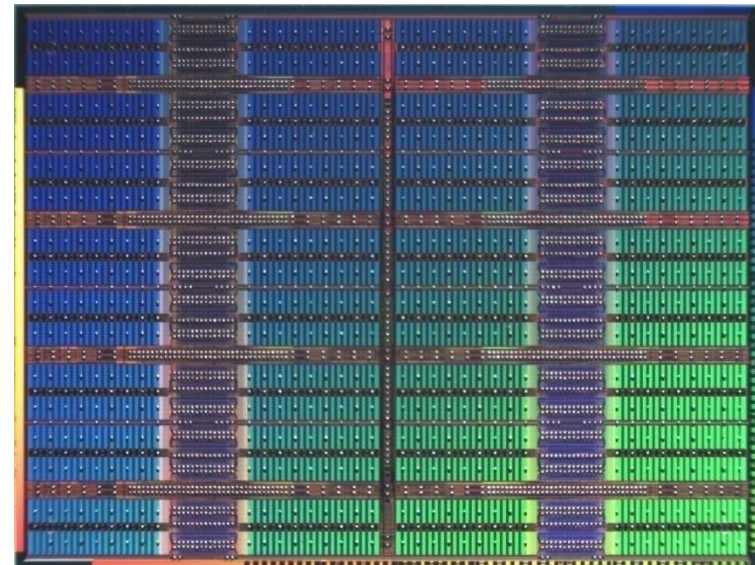
Technology	VDD	IDD	BW GB/s	Power (W)	mW/GB/s	pj/bit
SDRAM PC133 1GB Module	3.3	1.50	1.06	4.96	4664.97	583.12
DDR-333 1GB Module	2.5	2.19	2.66	5.48	2057.06	257.13
DDRII-667 2GB Module	1.8	2.88	5.34	5.18	971.51	121.44
DDR3-1333 2GB Module	1.5	3.68	10.66	5.52	517.63	64.70
DDR4-2667 4GB Module	1.2	5.50	21.34	6.60	309.34	38.67
HMC, 4 DRAM w/ Logic	1.2	9.23	128.00	11.08	86.53	10.82

Simple calculation from IDD7 (SDRAM IDD4)

Real system, some with lower density modules

- 1Gb DRAM Array
- 90nm prototype logic
- 512 MB total DRAM cube
- 128GB/s Bandwidth
- 27mm x 27mm prototype
- Functional demonstrations!

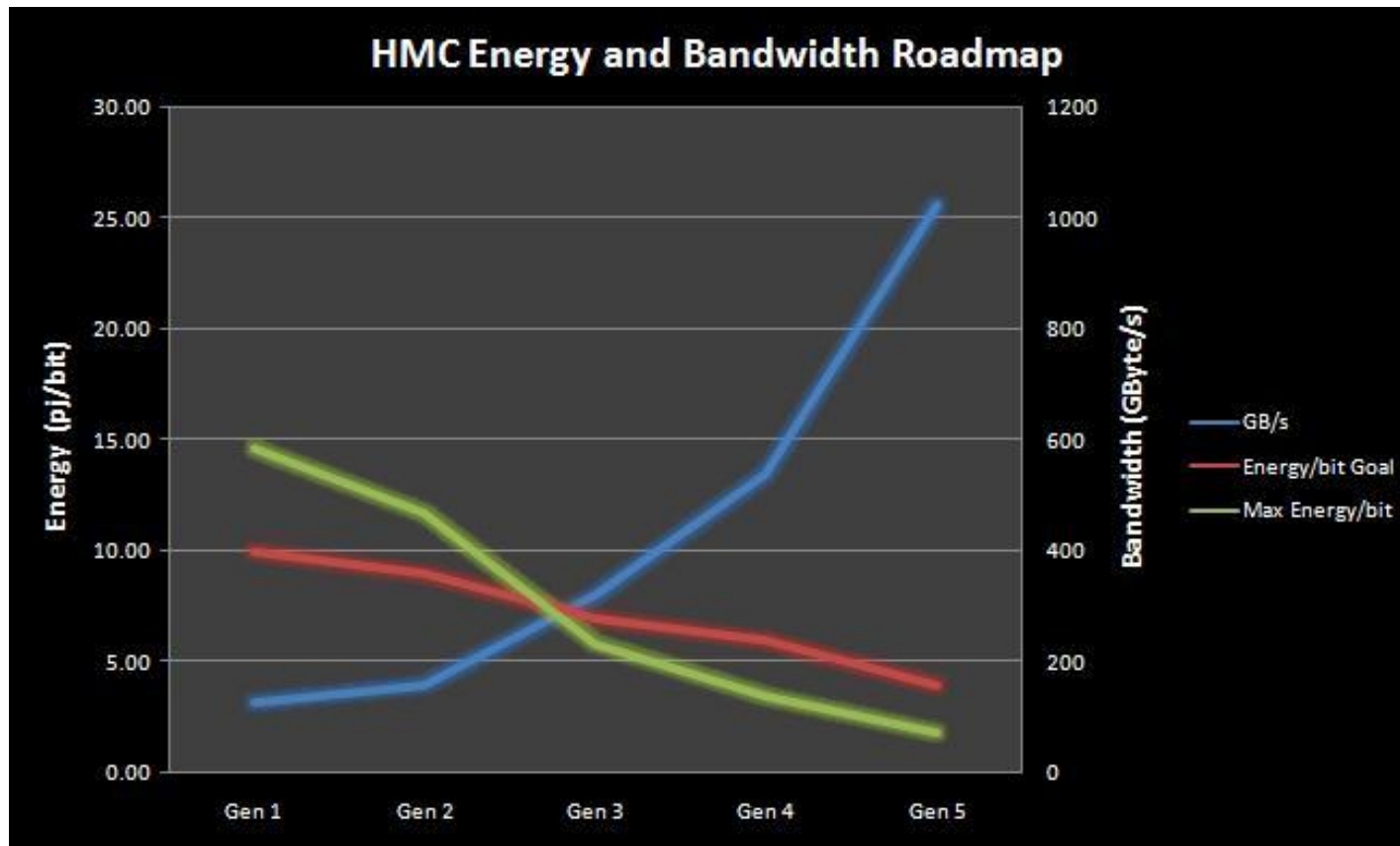
50nm prototype DRAM



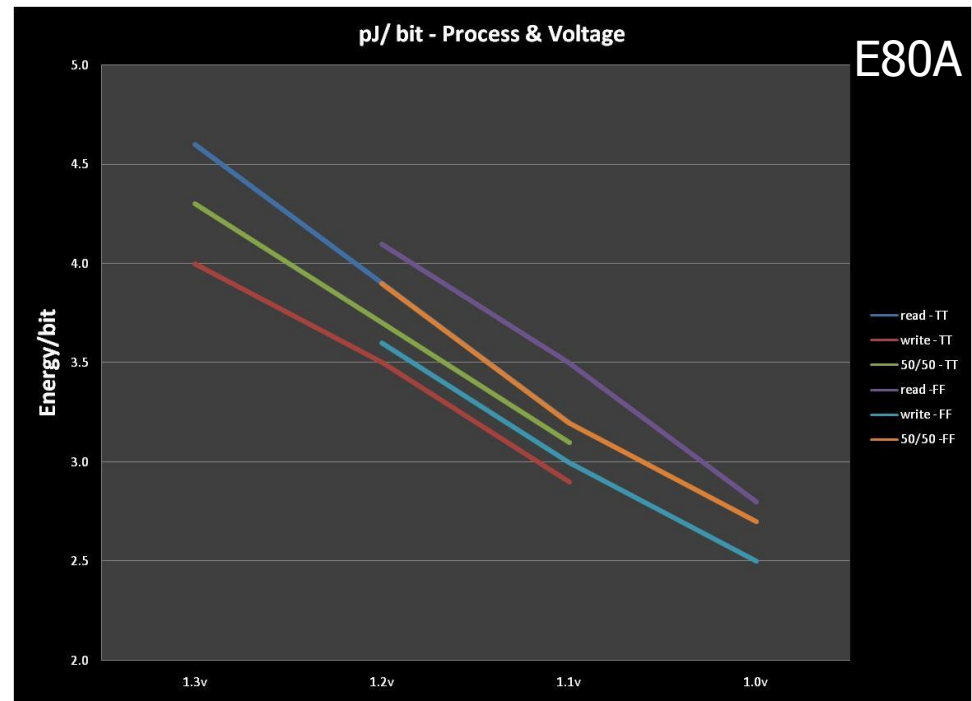
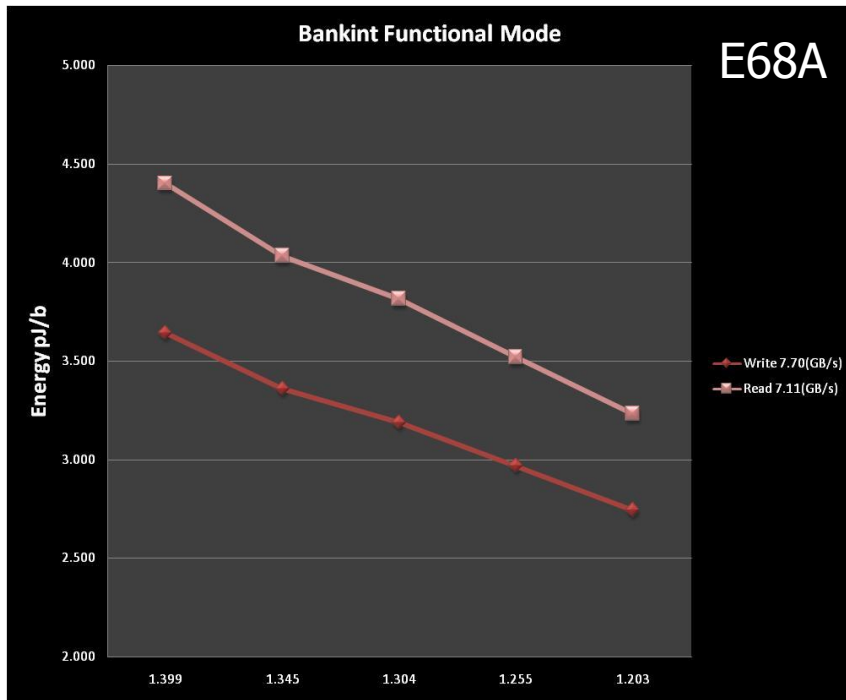
HMC Energy & Bandwidth Roadmap

	GB/s	Energy/bit Goal	Max Energy/bit
Gen 1	128	10.00	14.65
Gen 2	160	9.00	11.72
Gen 3	320	7.00	5.86
Gen 4	540	6.00	3.47
Gen 5	1024	4.00	1.83

15Watt Limit



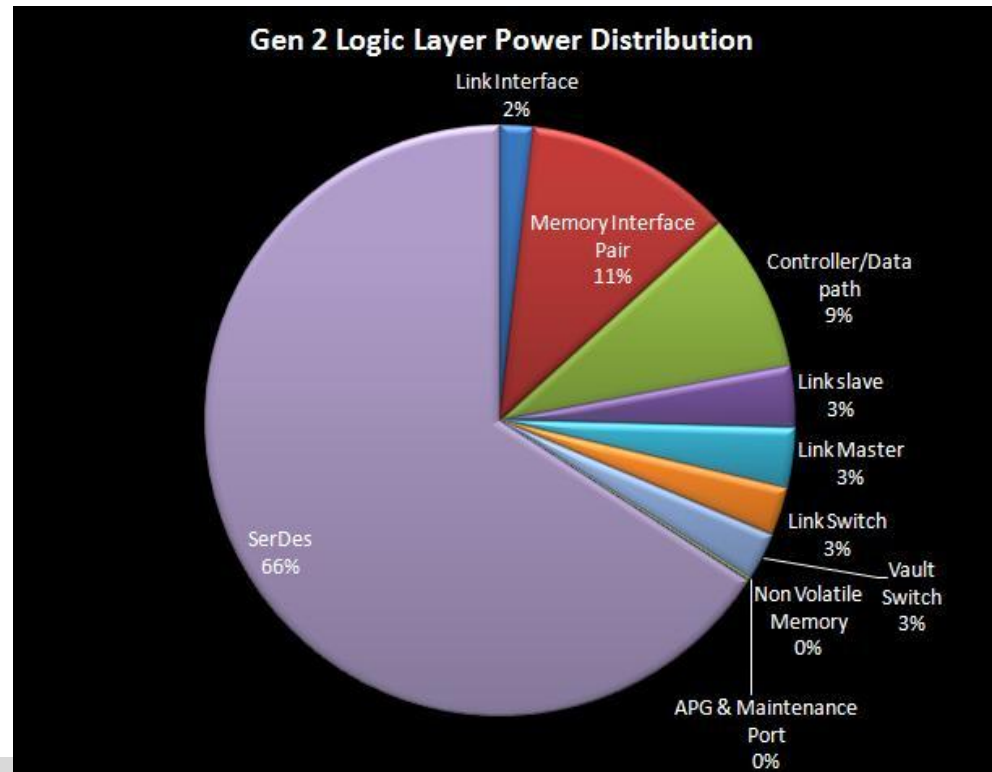
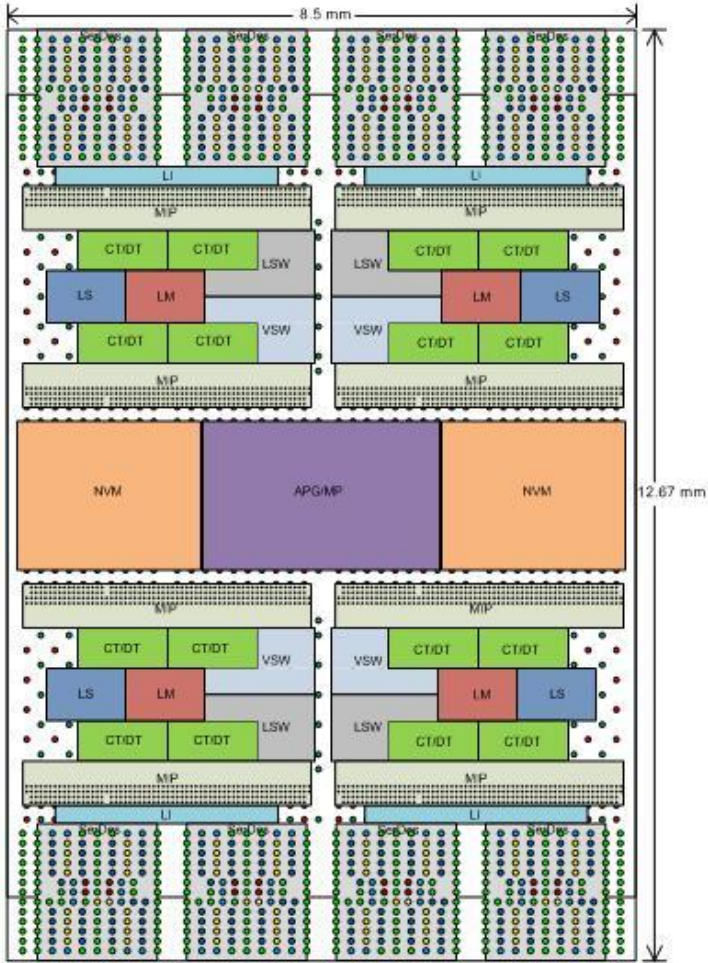
DRAM Voltage Scaling



- DRAM energy/bit is sensitive to supply voltage
- Process voltage scaling is important to reduce power.

Gen 2 Logic Energy Breakdown

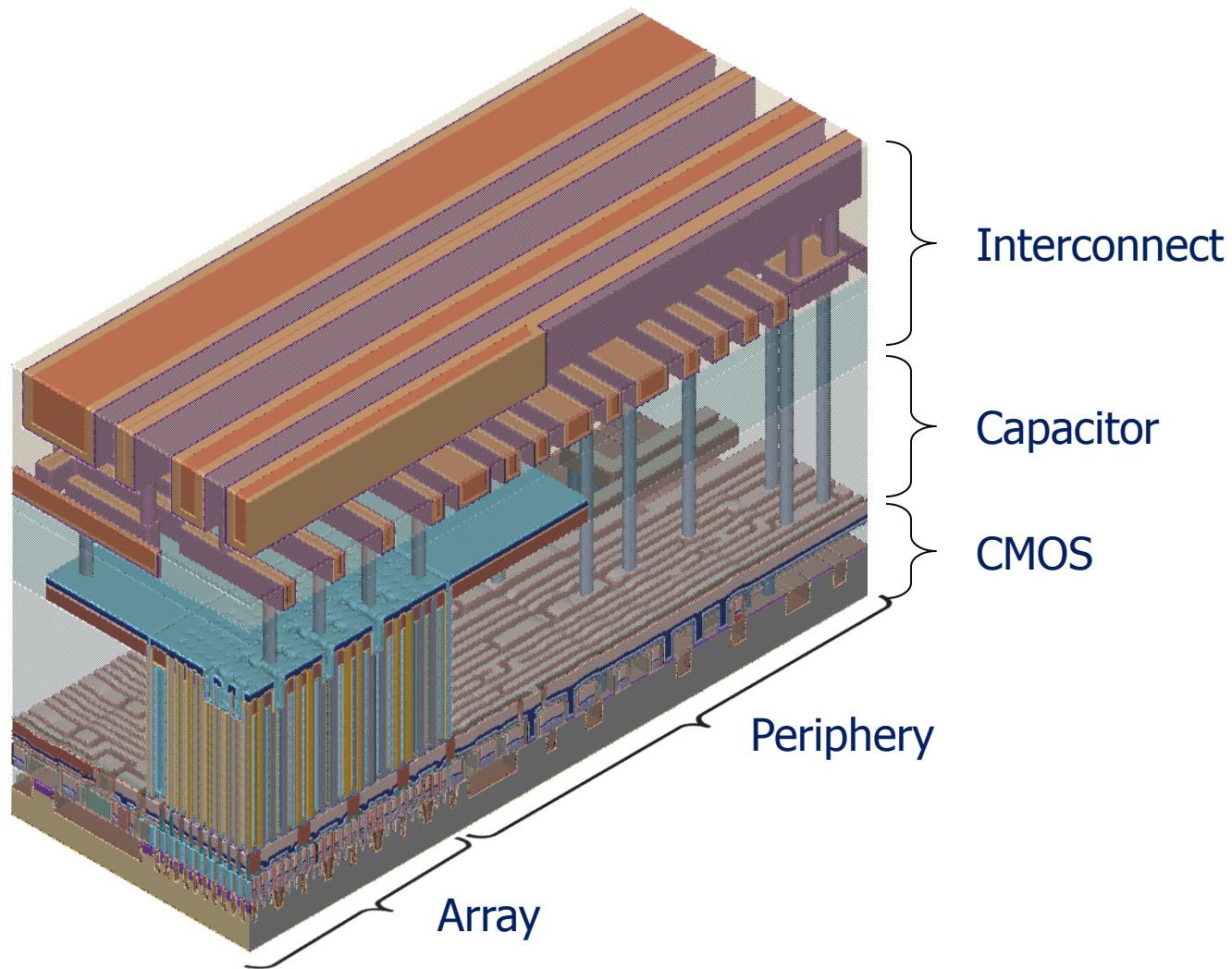
Description	Block
Link Interface	LI
Memory Interface Pair	MIP
Controller/Data path	CT/DT
Link slave	LS
Link Master	LM
Link Switch	LSW
Vault Switch	VSW
Non Volatile Memory	NVM
APG & Maintenance Port	APG/MP
SerDes	SerDes



Energy/bit Scaling

- The three most significant contributors to HMC energy consumption are the DRAM, the logic layer, and the host interface
- DRAM energy/bit needs to drop from one generation to the next
 - ▶ Gen 1: 4.7pj/bit
 - ▶ Gen 2: 4.0pj/bit
 - ▶ Gen 3: 2.3pj/bit
 - ▶ Voltage scaling is very important
- Logic layer energy consumption scales marginally with process
- Host interface energy consumption must scale to keep HMC on track

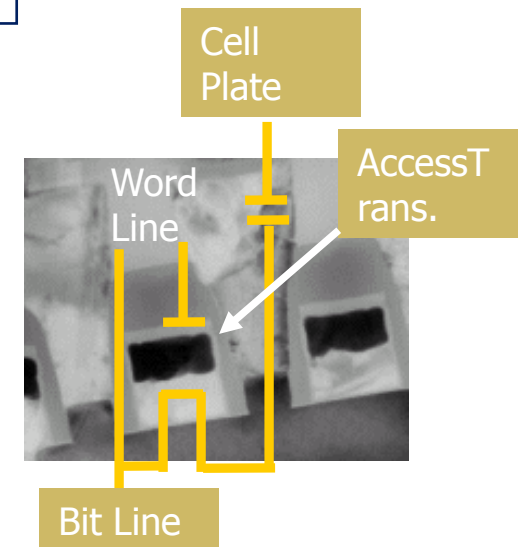
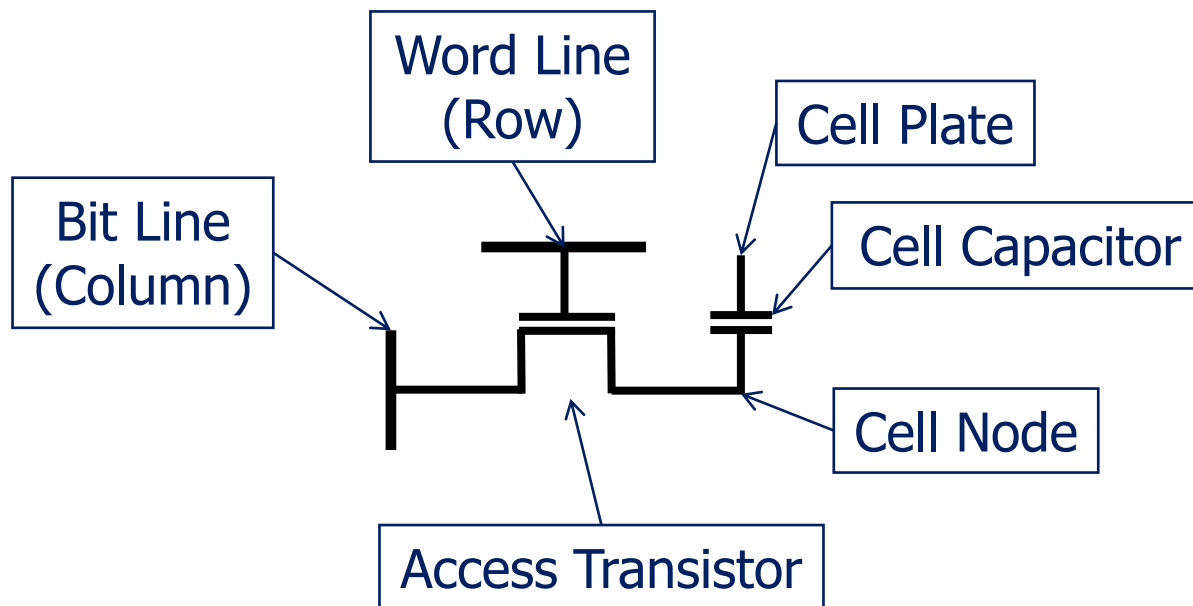
DRAM Isometric View



DRAM Access Device

Invented in 1968 – R. H. Dennard/IBM
US Patent# 3,387,286

1T/1C Cell



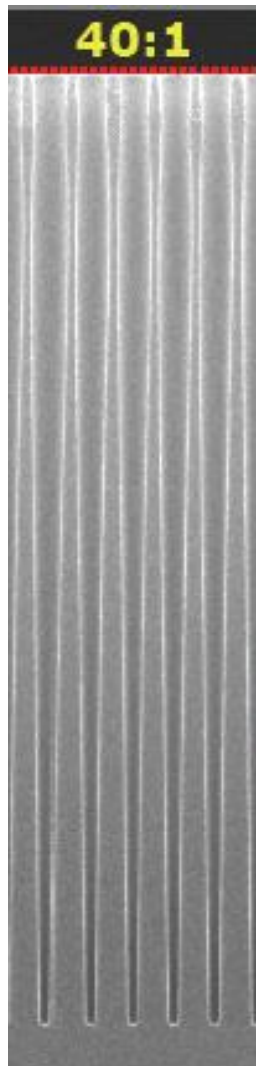
Typical specifications:
Cell Capacitance > 25 fF/cell
Leakage < 1 fA/cell

DRAM Capacitor Scaling

- Upcoming challenges for the DRAM capacitor
 - ▶ Cell cap requirement
 - High access device drive, low substrate leakage, low digit line cap → cell cap target = 18 fF/cell
 - ▶ Structural scaling
 - Aspect ratio limit for deep oxide etch (alternate materials)
 - Structural stability of lower electrode, support layers
 - Transition from container to post lower electrode
 - ▶ Dielectric scaling
 - K limit constrained by max thickness $\sim 100\text{\AA}$ due to structural scaling
 - Composition and morphology control in high aspect ratio structures

DRAM Capacitor Scaling

Double Sided
Container



High k dielectric Challenges

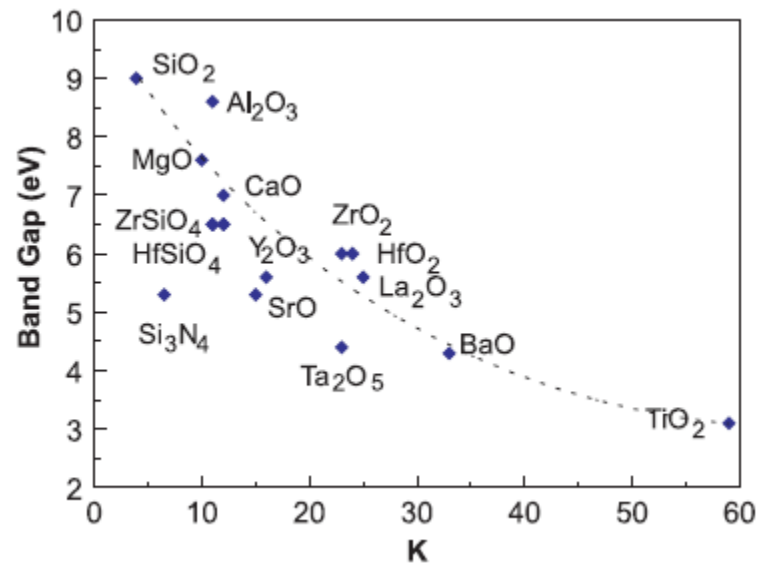
Lower band gap (offset)

Requires exotic metal electrodes

Crystallinity and defectivity

Optimize capacitance vs. leakage

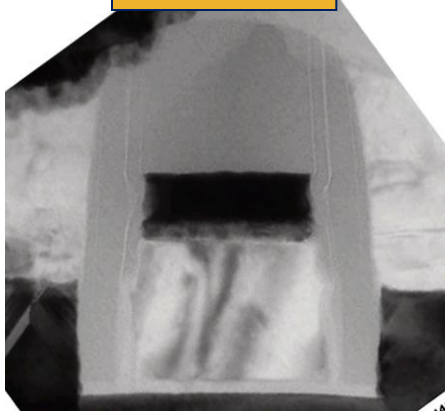
Dielectric relaxation



Access Device Structural Trends

- Device scaling → 3D structures → Process complexity
- Gate L gets smaller with Logic, “larger” with DRAM!

95nm



Planar Device

70nm



Recessed Device

5Xnm

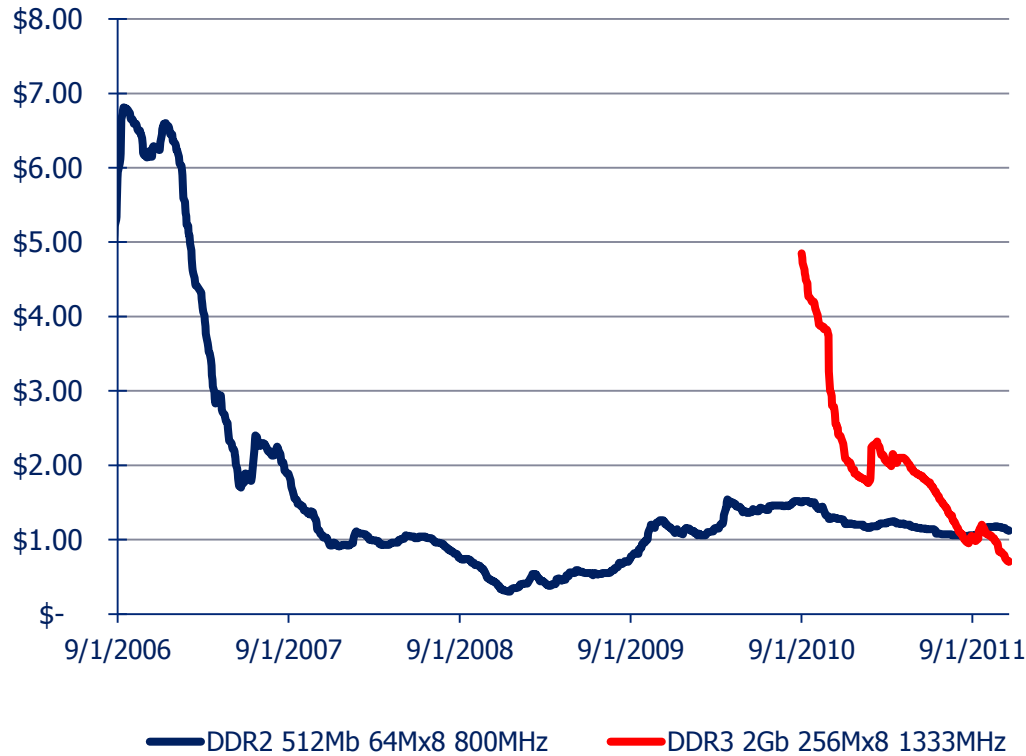


FinFET Device

- DRAM processing is optimized for cost and performance, including tradeoffs between periphery and array transistor devices
- Voltage scaling is slow due to need to maintain adequate signal to noise ratio

DRAM Price Trends

DRAM "Spot" Average Selling Price



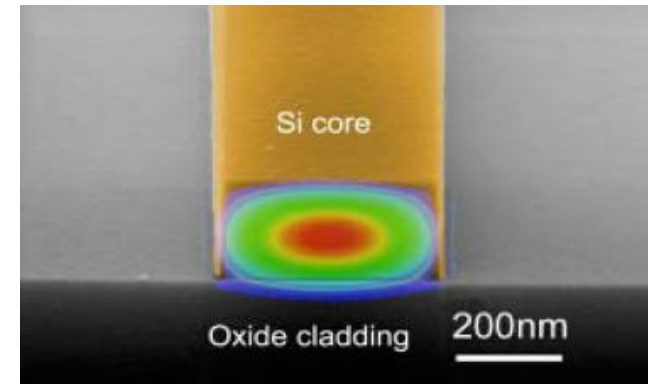
- Price vs. performance
- Economics matter

Source: DRAM Exchange



SOI for FEOL SiP Integration on DRAM

- Technical comments/questions
 - ▶ SOI has benefits for CMOS
 - ▶ Thin BOX sufficient for SiP?
 - ▶ Unclear benefits for advanced DRAM
- Economic comments/questions
 - ▶ SOI substrate costs significantly higher
 - ▶ Most CPU's (Intel) are fabricated on bulk wafers



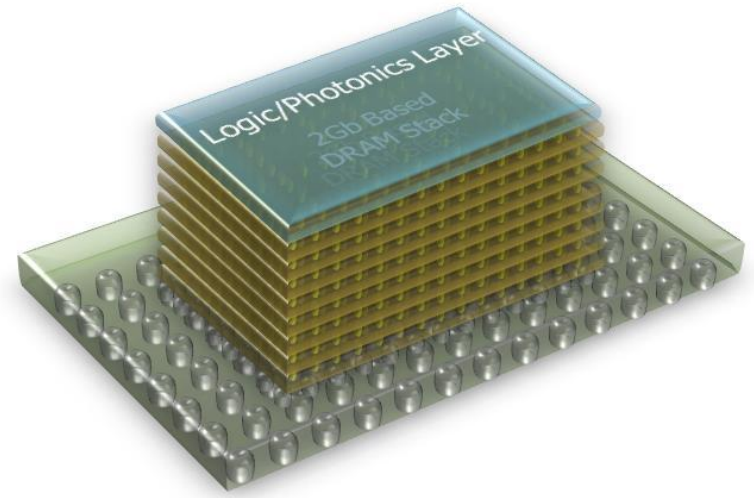
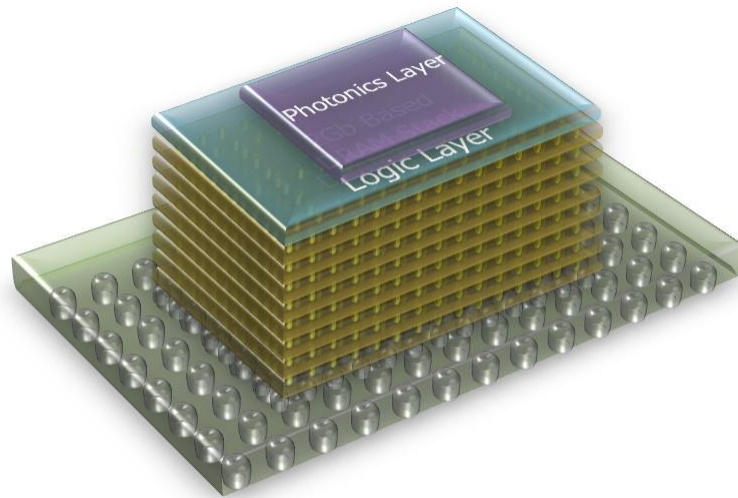
Source: IBM

Stand alone DRAM not likely to use SOI.

Summary so far...

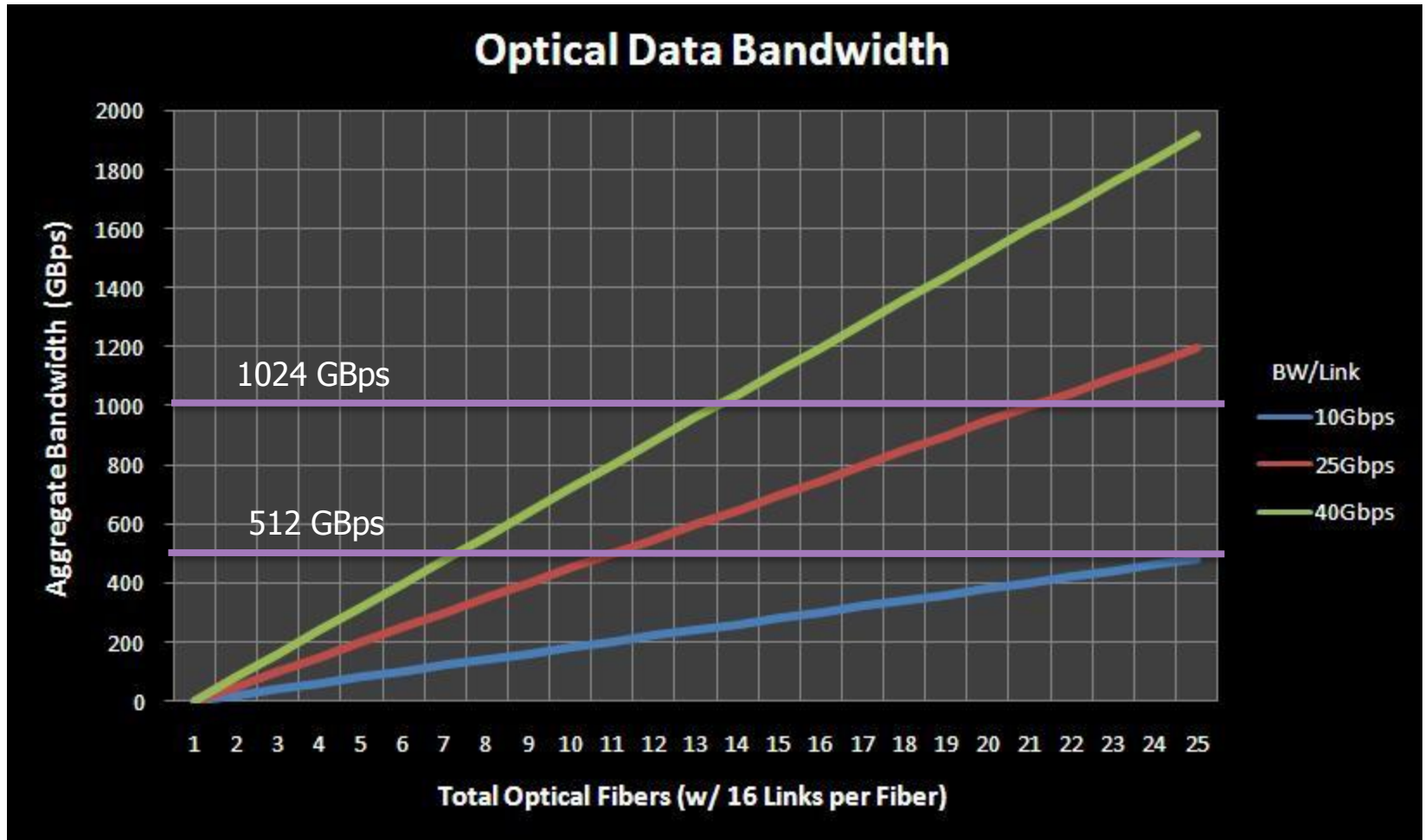
- Device power and ultimately energy/bit bound the maximum achievable bandwidth for each generation of HMC
- Process and voltage scaling contribute to a gradual lowering of energy/bit for the DRAM and logic layers
- Energy/bit of the host interface will not experience similar scaling
 - ▶ Laws of physics are non-negotiable
- Photonics may be the only path to 1TB/s

SiP Options for HMC



- HMC could benefit from SiP
- SiP options include separate logic and photonics, or
- Full integration of SiP onto logic layer

Aggregate Optical Data Bandwidth



Photonics Technology challenges

- Non SOI substrate based implementation
- Reduced material complexity
 - ▶ Si based detectors and modulators
 - ▶ Off chip light sources
- Technologies to enable simpler integration
 - ▶ Front end vs. Backend
 - ▶ Discrete photonic chip vs. fully integrated
- Non-Hermetic, SMT compatible Packaging solutions
 - ▶ Reliability, Cost, Alignment
- Design/Modeling/Simulation tools

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